

EEL 3712L LOGIC DESIGN I LAB

Final Exam – Fall, 2019 Instructor: Abdullah Aydeger

Student Name:

PID:

In order to get (partial) credit, please do not leave any step/question empty.

For the programming questions: If your code does not work, send all source code in .tex format to aaydeger@fiu.edu to get partial credits. (Do not expect to earn more than half points available).

Question 1: (30 points)

- (a) What are the names of the software, board, and programming language that we have used in the lab experiments? (4 points)
- (b) What are the necessary files to run a project on the board? What are their extensions? (3 points)
- (c) What are the necessary files to run a project in simulation environment? What are their extensions? (3 points)
- (d) Write the code that would appear after you create the following figure on software. (5 points)

Module Definition

Entity name:

Architecture name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
A	in	<input type="checkbox"/>	0	0
B	in	<input type="checkbox"/>	0	0
Cin	in	<input type="checkbox"/>	0	0
Cout	out	<input type="checkbox"/>	0	0
S	out	<input type="checkbox"/>	0	0

Buttons: ? OK Cancel

- (e) Write the following equation in the form of the programming language we used in the lab. Please pay attention to the syntax. You do not need to worry about the header and port definitions. (10 points)

$$\text{Cout} = \text{BACin} + \text{AB} + \text{Cin}$$

$$\text{S} = \text{AAB} + \text{CinBAB}$$

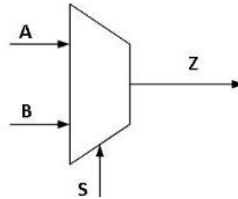
A,B,Cin,S,Cout are the variable names.

- (f) Make the truth table of Cout and S. (5 points)

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Question 2: (60 points)

- (a) What is a full-adder? Explain in short by showing its truth table. (3 points)
- (b) Write the equation for full-adder outputs in terms of inputs and draw the schematic. (7 points)
- (c) What is de-multiplexer? Explain in short by showing the truth table of 8 to 1 DEMUX. (7 points)
- (d) Draw the 8 to 1 DEMUX as a following box, showing all inputs and outputs. (3 points)



- (e) Draw the full schematic of 8 to 1 DEMUX using any logic gate(s) you need. (10 points)
- (g) Implement a **full-adder** in the simulation. **Make sure** to show the simulation screens working in the class to get a grade for this option. (30 points)

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Question 3: (10 + 40 points)

(a) In experiment 8, we implemented a 7-segment display (numbers on the board from 0-9). We have used the following code for that implementation. Please explain the reason behind this code. What does this code really do? (10 points)

```
a <=NOT((not I(2) and not I(0)) or (I(1) or (I(2) and I(0)) or (I(3))));
b<= NOT((not I(2)) or (not I(1) and not I(0)) or (I(1) and I(0)));
c <= NOT((not I(1)) or I(0) or I(2));
d <=NOT((not I(2) and not (I(0))) or (not I(2) and I(1)) or (I(2) and not I(1) and I(0)) or (I(1) and not I(0)) or (I(3)));
e <= NOT((not I(2) and not (I(0))) or ( I(1) and not (I(0))));
f <= NOT((not I(1) and not (I(0))) or ( I(2) and not (I(1)) or (I(2) and not (I(0)) or I(3)));
g <=NOT((not I(2) and (I(1))) or (I(2) and not (I(1))) or I(3) or (I(2) and not (I(0))));
```

Extra Part:

(b) Please implement 7-segment display code on the board such a way that board should display 4 when it is supposed to show 0. If you cannot implement in this way, you can implement a regular 7-segment display that we did in the experiment 8. Please notice that you will lose 20 points if you go with the second option. (40 points)

Hint: You will need to change the code given in the above screenshot in experiment 8.